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FIG. 3 is a circuit schematic diagram that corresponds to the monolithic power integrated circuit shown in FIG. 2. As explained previously, control circuit 21 may be selectively coupled to output transistor 23 or to output transistor 24, or to both transistors 23 & 24. This latter case is depicted by the dashed line showing a common connection to each of the three terminals (i.e., source, drain, and gate) of the respective output transistors. In one embodiment the output transistors are HVFETs that are connected in parallel to effectively act as a single HVFET which is switched on and off by the control circuit. In one embodiment the control circuit is a switching regulator circuit. Alternatively, the output transistors may have only one or two terminals coupled together (i.e., only the source terminals).

With reference now to FIG. 4, an alternative embodiment of an integrated circuit according to the present invention is shown including a control circuit 25 that occupies an L-shaped corner area of semiconductor die 20. In this embodiment, one outer side of the L-shaped area occupied by control circuit 25 has a length  $L_2$ , with the other outer side having a dimension substantially equal to the overall width ( $W \approx W_1 + W_2$ ) of semiconductor die 20. Output transistors 23 and 24 occupy an L-shaped area of die 20 adjacent to control circuit 25, such that die 20 has an overall rectangular shape with an aspect ratio within a range of 0.5 to 2.0. In this example, output transistor 23 is located adjacent the left-hand side of control circuit 25 and has a width  $W_1$  that is substantially equal to the width of the upper portion of control circuit 25. Either one (or both) of the output transistors 23 & 24 is coupled to control circuit 25. In FIG. 4 output transistor 24 is shown located beneath output transistor 23 and adjacent the upper inner side of control circuit 24. In this embodiment, the length of the transistor segments of output transistor 24 is less than the overall length of semiconductor die 20, which overall length ( $L$ ) is substantially equal to the sum of the length ( $L_1$ ) of output transistor 23 plus the length ( $L_2$ ) of the upper section of control circuit 25.

FIG. 5 shows yet another alternative embodiment of the present invention that includes a standardized control circuit 21 coupled to one or both of output transistors 27 and 28. In this embodiment, output transistor 28 occupies an area adjacent one side of control circuit 21 and has transistor segments substantially equal to a length  $L_1$ . Unlike the embodiment of FIG. 2, however, output transistor 28 has a much greater number of segments such that the width of transistor 28 is substantially equal to the overall width ( $W$ ) of semiconductor die 20. Output transistor 27 has a plurality of transistor segments, each of which has a length substantially equal to the length ( $L_2$ ) of control circuit 21. The width ( $W_2$ ) of output transistor 27 plus the width ( $W_1$ ) of control circuit 21 is substantially equal to the overall width ( $W$ ) of semiconductor die 20. Like the previous embodiments, control circuit 21 is selectively coupled to one or both of output transistors 27 & 28.

FIG. 6 illustrates an integrated circuit in accordance with still another alternative embodiment of the present invention. The embodiment of FIG. 6 includes an output transistor 27 disposed adjacent one side of control circuit 21, as in the embodiment of FIG. 5. The single output transistor 28 of FIG. 5, however, is replaced in FIG. 6 by a pair of output transistors 23 & 29 that occupy the same area adjacent the left-hand sides of transistor 27 and control circuit 21. Both transistors 23 & 29 have segments with substantially the same length ( $L_1$ ). Output transistor 23 has a width substantially equal to the width ( $W_1$ ) of control circuit 21. Output transistor 29 has a width substantially equal to the width ( $W_2$ ) of output transistor 27. In the embodiment of FIG. 6, control circuit 21 is coupled to one or more of transistors 23, 27, and 29, depending on the current handling capacity required. For example, in applications requiring maximum current handling capacity

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control circuit 21 would be coupled to all three transistors 23, 27, and 29. In cases where less than all of the output transistors are connected to control circuit 21, the unconnected output transistors may be available for use as independent transistors coupled to other off-chip circuitry.

Although the present invention has been described in conjunction with specific embodiments, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

I claim:

1. An integrated circuit (IC) comprising:

- a semiconductor die having a substantially rectangular shape with an aspect ratio within a range of 0.5 to 2.0;
- a control circuit occupying a first area of the semiconductor die, the control circuit having first and second sides, the first side being orthogonal to the second side;
- a first output transistor occupying a second area of the semiconductor die, the first output transistor having a first length that extends in a direction parallel to the first side;

- a second output transistor occupying a third area of the semiconductor die, the second output transistor having a second length that extends in a direction perpendicular to the second side, the second length being substantially equal to a difference between the first length and the length of the first side, the first length being at least 20% longer than a length of the first side of the control circuit; and

wherein the first and second output transistors each comprise field-effect transistors, each having source, drain, and gate terminals, the gate terminal of the first output transistor is coupled to the gate terminal of the second output transistor and to the control circuit.

2. The IC of claim 1 wherein the control circuit comprises a switched mode regulator control circuit.

3. The IC of claim 1 wherein the first and second output transistors comprise n-channel field-effect transistors.

4. The IC of claim 1 wherein the second area is disposed adjacent the first side, and the third area is disposed adjacent the second side.

5. An integrated circuit (IC) comprising:

- a semiconductor die of a substantially rectangular shape, the semiconductor die having an overall length and an overall width;

- a control circuit occupying a first area of the semiconductor die, the first area having first and second sides;

- one or more output transistors occupying an L-shaped second area of the semiconductor die, the L-shaped area having first and second inner sides that are respectively disposed adjacent the first and second sides of the first area, the first inner side having a length substantially equal to a length of the first side of the first area, the second inner side having a length substantially equal to a length of the second side of the first area, the L-shaped second area including first and second outer sides, the first outer side being substantially equal to the overall length of the semiconductor die, and the second outer side being substantially equal to the overall width of the semiconductor die; and

wherein at least one of the one or more output transistors is coupled to the control circuit.

6. The IC of claim 5 wherein the one or more output transistors comprise first and second output transistors each having source, drain, and gate terminals, the gate terminals of each of the first and second output transistors being coupled to control circuit.